

FDS4410

Single N-Channel Logic Level PWM Optimized PowerTrench™ MOSFET

General Description

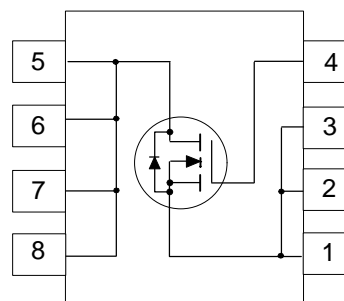
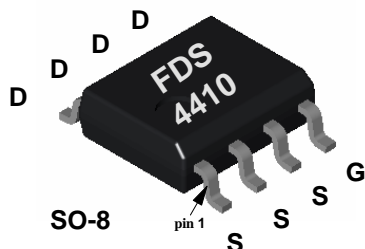
This N-Channel Logic Level MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers.

The MOSFET features faster switching and lower gate charge than other MOSFETs with comparable $R_{DS(ON)}$ specifications.

The result is a MOSFET that is easy and safer to drive (even at very high frequencies), and DC/DC power supply designs with higher overall efficiency.

Features

- 10 A, 30 V. $R_{DS(ON)} = 0.0135 \Omega$ @ $V_{GS} = 10$ V
 $R_{DS(ON)} = 0.0200 \Omega$ @ $V_{GS} = 4.5$ V.
- Optimized for use in switching DC/DC converters with PWM controllers.
- Very fast switching .
- Low gate charge (typical 22 nC).



Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless other wise noted

| Symbol | Parameter | FDS4410 | Units |
|----------------|--|------------|------------------|
| V_{DSS} | Drain-Source Voltage | 30 | V |
| V_{GSS} | Gate-Source Voltage | ± 20 | V |
| I_D | Drain Current - Continuous (Note 1a) | 10 | A |
| | - Pulsed | 50 | |
| P_D | Power Dissipation for Single Operation (Note 1a) | 2.5 | W |
| | (Note 1b) | 1.2 | |
| | (Note 1c) | 1 | |
| T_J, T_{STG} | Operating and Storage Temperature Range | -55 to 150 | $^\circ\text{C}$ |

THERMAL CHARACTERISTICS

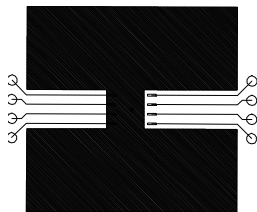
| | | | |
|-----------------|---|----|--------------------|
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient (Note 1a) | 50 | $^\circ\text{C/W}$ |
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case (Note 1) | 25 | $^\circ\text{C/W}$ |

Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

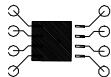
| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|-----|-------|--------|---------------|
| OFF CHARACTERISTICS | | | | | | |
| BV_{DSS} | Drain-Source Breakdown Voltage | $V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$ | 30 | | | V |
| $\Delta BV_{DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient | $I_D = 250\ \mu\text{A}$, Referenced to 25°C | | 21 | | mV/°C |
| I_{DSS} | Zero Gate Voltage Drain Current | $V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$ $T_J = 55^\circ\text{C}$ | | | 1 | μA |
| | | | | | 10 | μA |
| I_{GSSF} | Gate - Body Leakage, Forward | $V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$ | | | 100 | nA |
| I_{GSSR} | Gate - Body Leakage, Reverse | $V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$ | | | -100 | nA |
| ON CHARACTERISTICS (Note 2) | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$ | 1 | 2 | 3 | V |
| $\Delta V_{GS(th)}/\Delta T_J$ | Gate Threshold Voltage Temp. Coefficient | $I_D = 250\ \mu\text{A}$, Referenced to 25°C | | -4.5 | | mV/°C |
| $R_{DS(on)}$ | Static Drain-Source On-Resistance | $V_{GS} = 10\text{ V}, I_D = 10\text{ A}$ $T_J = 125^\circ\text{C}$ | | 0.011 | 0.0135 | Ω |
| | | | | | 0.018 | |
| | | $V_{GS} = 4.5\text{ V}, I_D = 9\text{ A}$ | | 0.017 | 0.02 | |
| $I_{D(on)}$ | On-State Drain Current | $V_{GS} = 10\text{ V}, V_{DS} = 5\text{ V}$ | 50 | | | A |
| g_{FS} | Forward Transconductance | $V_{DS} = 10\text{ V}, I_D = 10\text{ A}$ | | 27 | | S |
| DYNAMIC CHARACTERISTICS | | | | | | |
| C_{iss} | Input Capacitance | $V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$ | | 1340 | | pF |
| C_{oss} | Output Capacitance | | | 340 | | pF |
| C_{rss} | Reverse Transfer Capacitance | | | 125 | | pF |
| SWITCHING CHARACTERISTICS (Note 2) | | | | | | |
| $t_{D(on)}$ | Turn - On Delay Time | $V_{DS} = 15\text{ V}, I_D = 1\text{ A}$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\ \Omega$ | | 12 | 22 | ns |
| t_r | Turn - On Rise Time | | | | 13 | 24 |
| $t_{D(off)}$ | Turn - Off Delay Time | | | 38 | 60 | ns |
| t_f | Turn - Off Fall Time | | | | 10 | 18 |
| Q_g | Total Gate Charge | $V_{DS} = 15\text{ V}, I_D = 10\text{ A},$ $V_{GS} = 10\text{ V}$ | | 22 | 31 | nC |
| Q_{gs} | Gate-Source Charge | | | | 5 | nC |
| Q_{gd} | Gate-Drain Charge | | | | 4 | nC |
| DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS | | | | | | |
| I_S | Maximum Continuous Drain-Source Diode Forward Current | | | | 2.1 | A |
| V_{SD} | Drain-Source Diode Forward Voltage | $V_{GS} = 0\text{ V}, I_S = 2.1\text{ A}$ (Note 2) | | 0.73 | 1.2 | V |

Notes:

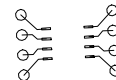
- $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 50°C/W on a 1 in^2 pad of 2oz copper.



b. 105°C/W on a 0.04 in^2 pad of 2oz copper.



c. 125°C/W on a 0.006 in^2 pad of 2oz copper.

Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

Typical Electrical Characteristics

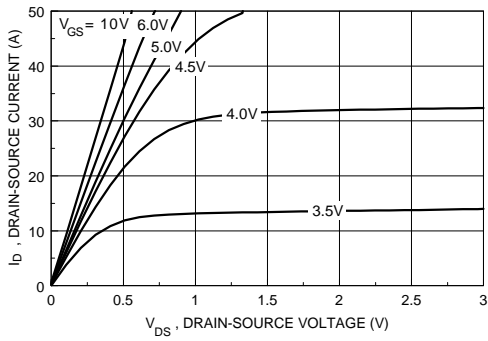


Figure 1. On-Region Characteristics.

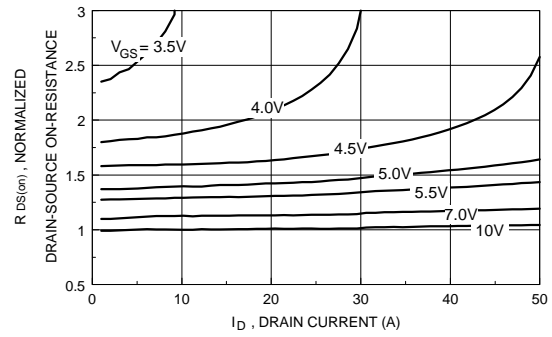


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

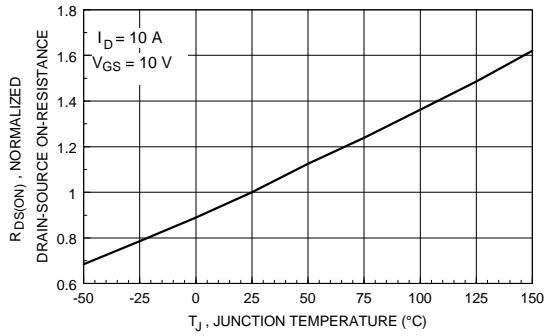


Figure 3. On-Resistance Variation with Temperature.

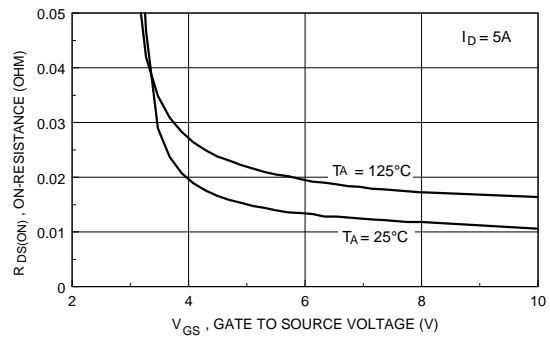


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

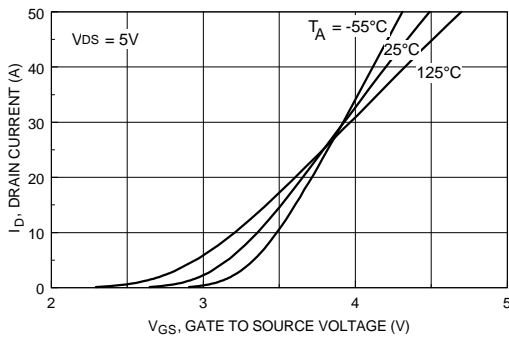


Figure 5. Transfer Characteristics.

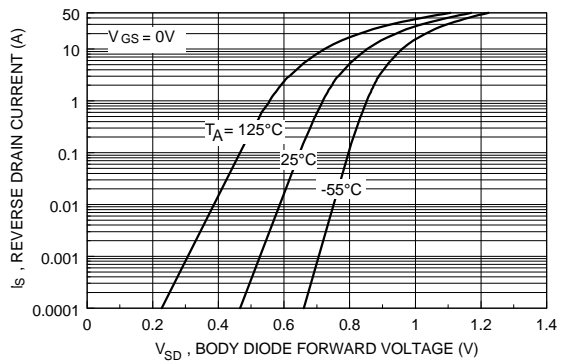


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Electrical And Thermal Characteristics

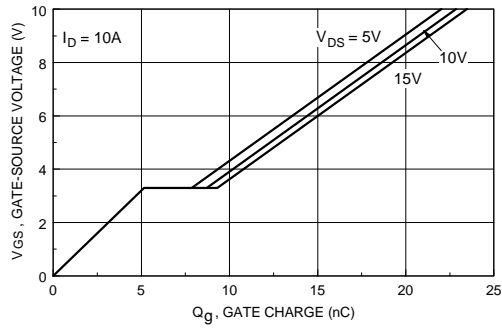


Figure 7. Gate Charge Characteristics.

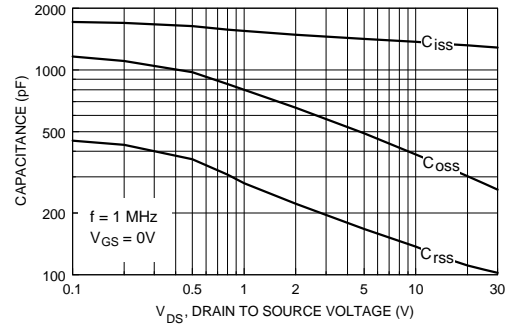


Figure 8. Capacitance Characteristics.

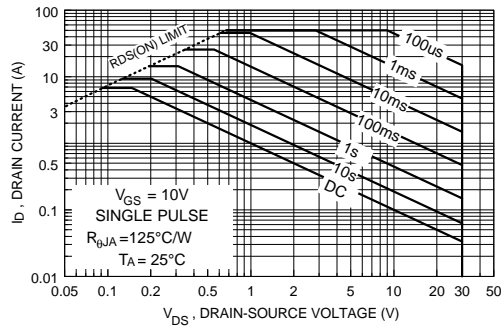


Figure 9. Maximum Safe Operating Area.

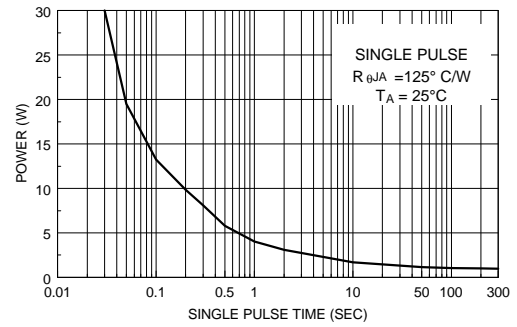


Figure 10. Single Pulse Maximum Power Dissipation.

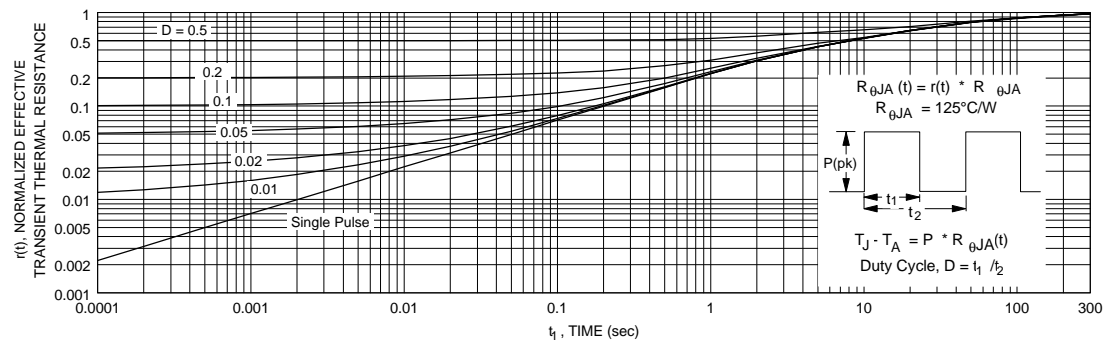


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.

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